# METHOD AND SYSTEM FOR SUPPORTING MULTIPLE CACHE CONFIGURATIONS

## ABSTRACT OF THE DISCLOSURE

A processor card for supporting multiple cache configurations, and a microprocessor for selecting one of the multiple cache configurations is disclosed. The processor card has a first static random access memory mounted on a front side thereof and a second static random access memory mounted on a rear side thereof. The address pins of the memories are aligned. Each pair of aligned address pins are electrically coupled to thereby concurrently receive an address bit signal from the microprocessor. During an initial boot of the microprocessor, the microprocessor includes a multiplexor for providing the address bit signals to the address pins in response to a control signal indicative of a selected cache configuration.